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Ka-BAND GaAs POWER FETs

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ABSTRACT

Ka-band results using submicrometer gate length, air-bridged, and soldered flip-chip GaAs power FETs in finline and ridge-waveguide circuits are reported. Conventional photolithography was used to fabricate FETs with submicrometer gate lengths by using the undercut associated with chemical etching. At 35 GHz an output power of 91 mW at 3 dB gain and 4.5% efficiency was measured.

INTRODUCTION

This paper describes submicrometer (0.5-0.7 μm) gate length planar GaAs FETs that generate output power as high as 91 mW at 35 GHz with 3 dB power gain and 4.5% power-added efficiency. The GaAs FETs are in the flip-chip configuration to minimize thermal resistance and parasitic source inductance. The submicrometer gate length is obtained using conventional contact photolithography and the undercut associated with chemical etching.[1,2]

DEVICE DESIGN AND FABRICATION

Devices were fabricated from both ion-implanted and epitaxially-grown GaAs wafers. Ion implantation of Si (50 and 190 keV) was done directly into qualified SI GaAs substrates. The implanted substrates were capless annealed under arsenic overpressure at 825°C for 20 minutes. Epitaxial layers were grown by the hydride VPE technique and were either Se or Te doped. Typical active layer doping was in the $1\text{-}2\text{x}10^{17}\text{cm}^{-3}$ range.

The cross-section of the typical device is shown in Fig. 1. Note that a T-shaped gate structure is used to obtain submicrometer gate length while keeping the gate metallization resistances from increasing. Two basic device configurations are being evaluated. The first configuration has a cell width of 600 μm with a unit gate stripe width of 150 μm[1,2]. Each GaAs FET pellet has four 600 μm cells. The second configuration consists of a unit gate stripe width of 75 μm. Unit cells of 150, 300, and 600 μm gate width are provided to investigate the influence of cell size on Ka-band performance.

The fabrication process is described in detail in reference 2. The main process steps are as follows. Ohmic contacts of AuGe/Ni/Au are formed by liftoff patterning and sintered in forming gas for 60 s at 450°C. Active device areas are then defined by chemically etching mesas. Device currents are adjusted by etching a double gate recess in a channel with a 4.5 μm source-drain separation. The depth of the smaller gate recess is about 0.1 μm to increase the gate-to-drain breakdown voltage.[3,4]

A two-layer photoresist technique is used to produce a pattern with an undercut profile for gate metal deposition.[5] The top resist layer is patterned with a 1 μm gate opening by contact photolithography. A Ti/Pt/Au gate with a nominal 1 μm gate length is produced by liftoff. The Ti layer is then chemically etched laterally to reduce the gate metal length to submicrometer dimensions. Figure 2 is an SEM of a gate produced by this process. All the GaAs under the gate has been etched away to facilitate SEM examination. The gate in Fig. 2 is shown upside down with the 0.5 μm Ti layer on top. The lack of raggedness of the Ti layer edge attests to the good control obtained with this technique. Device fabrication is completed by electroplating 10-15 μm of Au on the source contacts and the gate and drain pads. The sources are then interconnected by continuing the Au plating selectively in the source area using the mushrooming effect of dc electroplating to bridge the gap between the sources. Figure 3 is an SEM showing details of the air-isolated source bridge. The major advantage of this bridged structure is that it allows soldering of the device to a carrier thereby improving thermal resistance and improving the grounding of the sources.

Ka-BAND TEST CIRCUITS

Low-loss Ka-band finline and ridge waveguide test fixtures were developed. Both fixtures have input and output waveguide-to-microstrip transitions and a central microstrip section to hold the device carrier and to allow tuning using chips.

The finline test fixture is shown in Fig. 4. A double-sided pattern is printed on 0.254 mm thick Duroid and the board is soldered into the test fixture. The pattern is similar to that used by Lavedan[6] and by VanHewen.[7] The biases are brought in through three-section quarter-wave filters printed on the pattern. The chip resistor in the gate bias line is used to suppress oscillations. With bias lines and dc blocking series beam lead capacitors (not shown) and a through microstrip line instead of a device, the test fixture has less than 1.2 dB insertion loss from 28 GHz to 36 GHz.

A photograph of the ridge waveguide fixture is shown in Fig. 5. Bias injection for the FET is provided through the ridges that are dc-isolated from the waveguide wall. The electrical characteristics of the transition is very dependent upon the ridge geometry and ridge-to-microstrip connection point. The broadest bandwidth results were obtained with a stepped ridge design where the fixture had an insertion loss of 1.2 dB over the 26.5 to 40.0 GHz range. Lower loss (0.75 dB) was obtained over the 27 to 35 GHz band.

The devices were tuned by several techniques. The device is first solder-flipped onto the pedestal of a carrier and the gate and drain leads bonded to ceramic standoffs. The standoffs are patterned to allow some on-carrier lumped-element impedance matching. The device is further tuned by placing chips on the microstripline. The ridge waveguide fixture has periodically spaced dielectric rods in the waveguide section for additional tuning. External waveguide E-H and slide-screw tuners have not been as useful. The best device results to date were obtained with on-carrier prematching and using tuning chips on the microstripline in the finline fixture.

RESULTS

Figure 6 summarizes the best narrow-band tuned output power and efficiency at 3 dB gain in the 26-35 GHz frequency range. The results at 27, 30, and 32.5

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GHz were obtained from a 300 μm wide cell with 75 μm gate stripe width. At 35 GHz an output power of 91 mW at 3 dB gain and 4.5% power-added efficiency was obtained with a 600 μm cell that has a 150 μm unit gate stripe width. The reported results include fixture losses. The output power per mm of gate width varies from 0.32 to 0.15 W/mm.

Some devices have also been tuned over broader bandwidths. The circuit used to tune one device at 35 GHz is shown in Fig. 7. The device leads and the carrier standoffs are considered as microstriplines for computer modelling. Conceptually, the low-impedance standoffs act to rotate the device's characteristics to the points where a series inductance matches the gate impedance while a shunt capacitance followed by a series inductance 120° later matches the drain impedance. The initial design was based on S-parameters extrapolated from the 11-18 GHz S-parameter measurements. The amplifier was then constructed empirically.

The device in the test fixture showed at least 3 dB gain between 34.5 and 36.0 GHz. The gains at several input power levels as functions of frequency are shown in Fig. 8. The device had a 1.0 GHz bandwidth for 3 dB gain at 45 mW output power.

The test results for devices from several different wafers are summarized in Table 1. The fixture losses are not separated from the reported results.

CONCLUSIONS

Submicrometer gate length flip-chip GaAs FETs that operate at Ka-band have been developed and evaluated in low-loss finline and ridge waveguide test structures. An output power of 91 mW with 3 dB gain and 4.5% power-added efficiency was realized. The best efficiency obtained was 4.8% with 4.3 dB power gain and 80 mW output power at 35 GHz. These data include test fixture losses.

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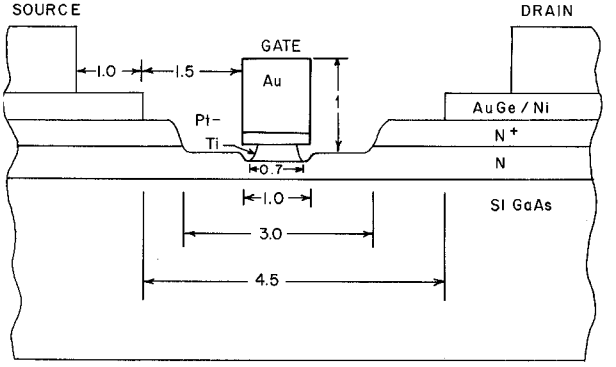

Fig. 1. GaAs FET cross-section.

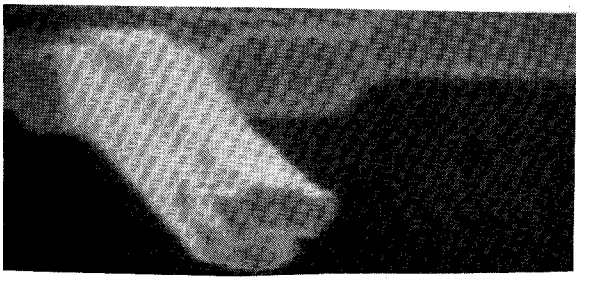

Fig. 2. SEM of gate from underneath (20 kX). Ti layer on top.

TABLE 1. Ka-Band Test Results

Wafer/Device Number	Unit Gate Stripe Width (μm)	Cell Width (μm)	Frequency (GHz)	At 3 dB Gain P_o(mW)	η_{PA}(%)	W/mm
B1499 #98	150	600	35	91	4.5	0.15
#139	"	"	"	64	3.1	0.11
#137	"	"	"	69	3.6	0.12
#136	"	"	"	76	4.2	0.13
B1692 #3B	75	300	27	81	5.8	0.27
"	"	"	30	70	4.5	0.23
"	"	"	32.5	94	6.0	0.31
"	"	"	35	36	2.6	0.12
E37T* #8A	75	150	27	21	5.5	0.18
E6* #A	"	"	"	31	5.4	0.21

*Ion implanted wafers.

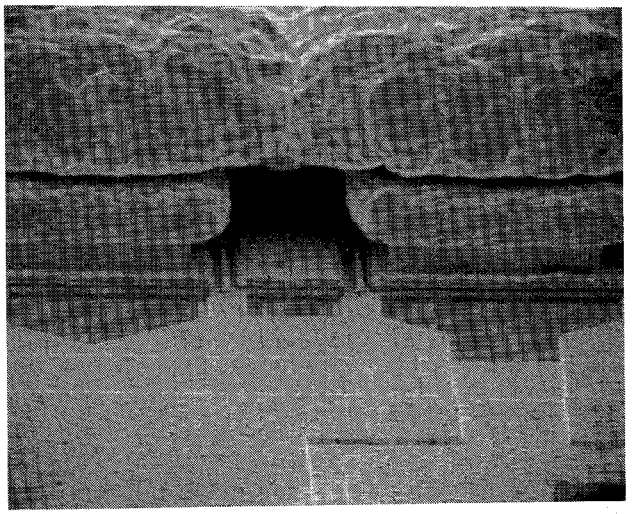

Fig. 3. SEM of GaAs FET - air-isolated source bridge.

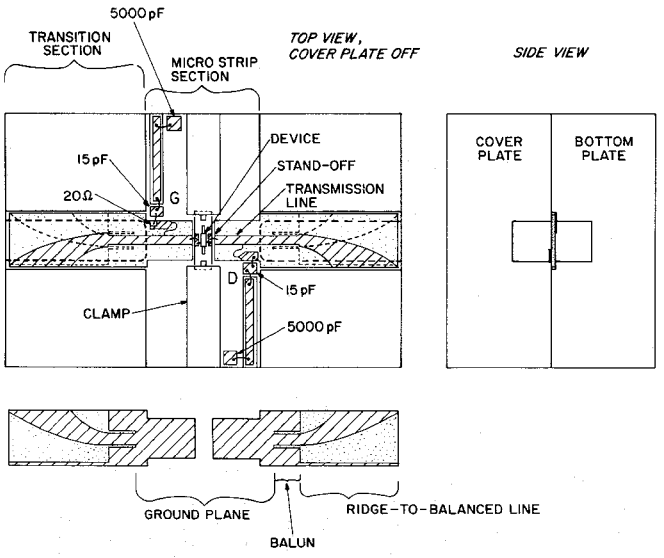

Fig. 4. Ka-band fin-line test fixture.

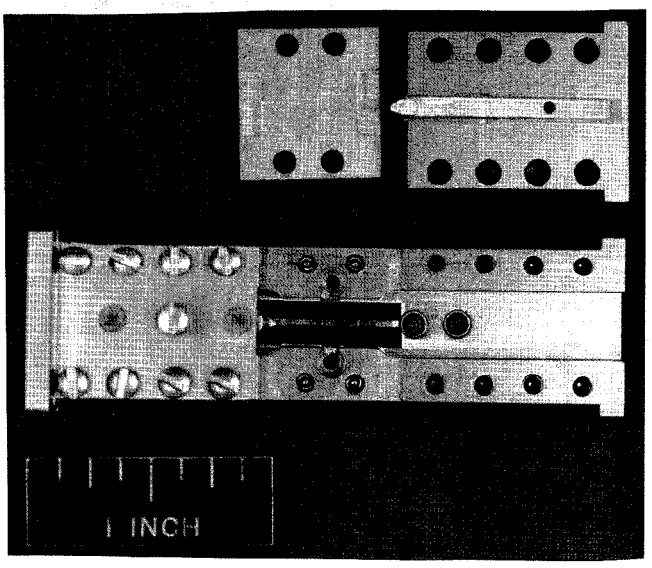

Fig. 5. Ka-band ridge waveguide test fixture.

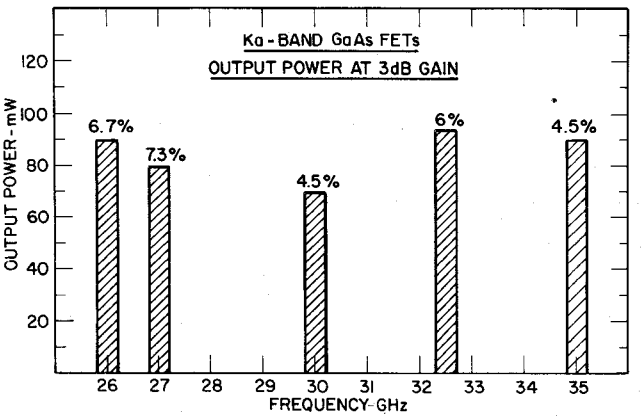

Fig. 6. Narrow-band Ka-band performance.

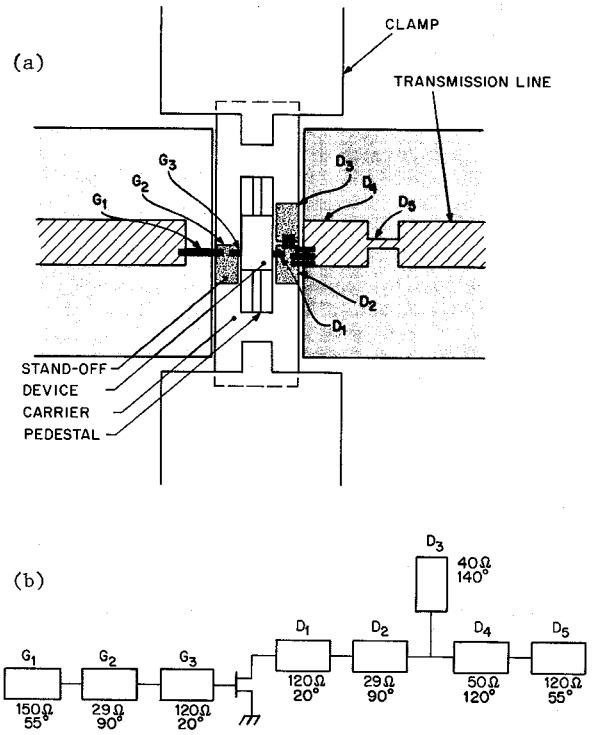

Fig. 7a. Matching circuit at 34.5-36.0 GHz.
7b. Equivalent transmission-line circuit.

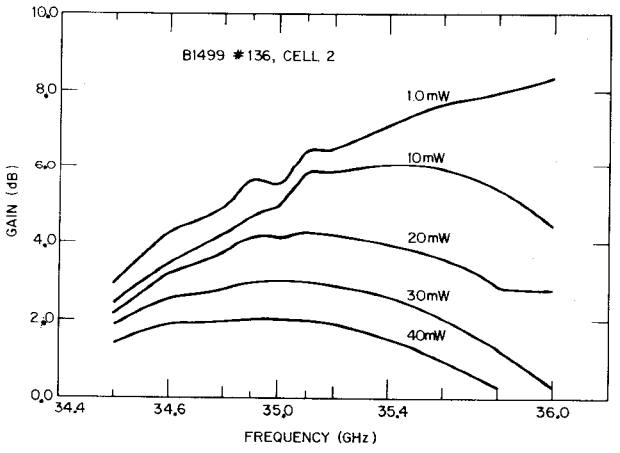

Fig. 8. Performance of circuit shown in Fig. 7. Input power as parameter.